

James (Hyung Suk) Yang

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SUMMARY: 2nd year Ph.D. candidate at Georgia Tech with eight refereed publications. Research topics include modeling, fabricating, testing and characterizing interconnect and packaging technologies required for heterogeneous 3D integration of CMOS and MEMS/Sensors.

EDUCATION:

Georgia Institute of Technology, Atlanta, GA

Ph.D. in Electrical and Computer Engineering

Jan. 2009 – Dec. 2012 (expected)

- Thesis Topic: Heterogeneous 3D Integration of CMOS and MEMS/Sensors
- Advisors: Dr. James D. Meindl and Dr. Muhannad S. Bakir
- Qualifier examination passed

M.S. in Electrical and Computer Engineering (GPA: 3.70/4.00)

Aug. 2007 – Dec. 2008

- Certificate in Microsystems Packaging from PRC
- Minor in Management

B.S. in Computer Engineering w/ High Honor (GPA: 3.42/4.00)

May 2003 – Aug. 2007

RELATED EXPERIENCE:

GigaScale Integration (GSI) Group, Graduate Research Assistant Jan. 2008 – Present

- Developed fabrication processes for microfluidic channels, compliant I/Os and TSVs
- Developed assembly processes for 3D integrated systems w/ compliant I/Os
- Performed mechanical/electrical modeling, testing and characterizations
- Trained users for STS ICP (DRIE), X-ray tomography, flipchip bonder and probe station
- Collaborated with various companies incl. TI, Oracle, Freescale and SRC

AWARDS/HONORS:

- 2010 Georgia Tech Research and Innovation Conference Outstanding Poster Presentation Award
- 2009 IMAPS International Symposium on Microelectronics Best Student Paper Award
- 2009 IMAPS International Symposium on Microelectronics Best in Session Paper Award
- 2009 SRC TECHCON Best in Session Paper Award
- Member of Eta Kappa Nu – held corresponding secretary position
- Member of Omicron Delta Upsilon (Economics Honor Society)
- Member of National Society of Collegiate Scholars (NSCS)

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PUBLICATIONS:

Refereed Journal

[1] J. H. Lai, **H. S. Yang**, H. Chen, C. R. King, J. Zaveri, M. S. Bakir, "Improved Through-Silicon-Via Fabrication for Thick Wafers Containing MEMS/Sensor Devices," Journal of Microelectronics Engineering, 2009

Refereed Conference Proceedings

[1] J. Zaveri, C. R. King, **H. S. Yang**, M. S. Bakir, "Wafer Level Batch Fabrication of Silicon Microchannel Heat Sinks and Electrical Through Silicon Vias," SRC TECHCON, Austin, TX, Sept. 2009.

[2] C. R. King, J. Zaveri, **H. S. Yang**, M. S. Bakir, J. D. Meindl, "Electro-Fluidic C4 Interconnections for Inter-Layer Liquid Cooling of 3D ICs," SRC TECHCON, Austin, TX, Sept. 2009.

[3] J. Zaveri, C. R. King, **H. S. Yang**, M. S. Bakir, "Wafer Level Batch Fabrication of Silicon Microchannel Heat Sink and Electrical Through-Silicon Vias for 3D ICs", IMAPS 42nd International Symposium on Microelectronics, San Jose, CA Nov. 2009.

[4] **H. S. Yang**, M. S. Bakir, "Interconnect Technologies for 3D Integration of CMOS and MEMS," Proc. MRS Spring Meeting, San Francisco, CA April 2010. **(INVITED)**

[5] **H. S. Yang**, M. S. Bakir, "Mechanically Flexible Interconnects with High Out-of-Plane Range-of-Movement and Thick Wafer Through Silicon Vias for CMOS and MEMS Integration," IEEE 60th Electronic Components and Technology Conference, Las Vegas, NV June 2010.

[6] R. Ravindran, J. A. Sadie, K. E. Scarberry, **H. S. Yang**, M. S. Bakir, J. F. McDonald, and J. D. Meindl, "Biochemical Sensing with an Arrayed Silicon Nanowire Platform," IEEE 60th Electronic Components and Technology Conference, Las Vegas, NV June 2010.

[7] **H. S. Yang**, M. Bakir, "A 3D Interconnect System for Large Biosensor Array and CMOS Signal-Processing IC Integration," IEEE International Interconnect Technology Conference, San Francisco, CA June 2010.

RELATED COURSEWORK:

Microsystems

IC Fabrication, Semiconductor Process Control, Electronic Packaging Assembly, Microelectronic Systems Packaging, Integrated Optics

Computer Engineering

Physical Design Automation, Advanced VLSI Systems, Digital Systems Test, Internetwork Programming, Computer Languages and Translations, Computer Architecture, Low Noise Electronics

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SKILLS:

Microsystems Fabrication Skills

- **Processing Equipments:** Photolithography tools, sputtering, electron-beam evaporation, metal electroplating (Ni, Cu, Au, Solder), Plasma Enhanced Chemical Vapor Deposition (PECVD), Reactive Ion Etching tools (RIE), wet chemical etching, wafer to wafer bonding, Chemical-Mechanical Planarization (CMP), flipchip bonding
- **Characterization Tools:** Scanning Electron Microscope (SEM), refractometry, contact profilometry, X-ray tomography

Design, Layout, and Simulation Software

- Microsystems (CMOS, MEMS etc) mask design experience
- ANSYS Workbench FEM modeling and simulations
- MATLAB, MathCAD, SPICE, Cadence Virtuoso, Mentor Calibre

Computer Skills

- IT Certifications: MCSE, MCSA, MCDBA, CCNA, CIW Associate
- Software Engineering: C, C++, C#, JAVA, ASP.NET, SQL, IIS, Python,

Other

- Expert-level skier
- Certified skydiver w/ ~100 jumps
- Fluent in Korean and English
- IRB certified